Field-Programmable Gate Array

Technology overview

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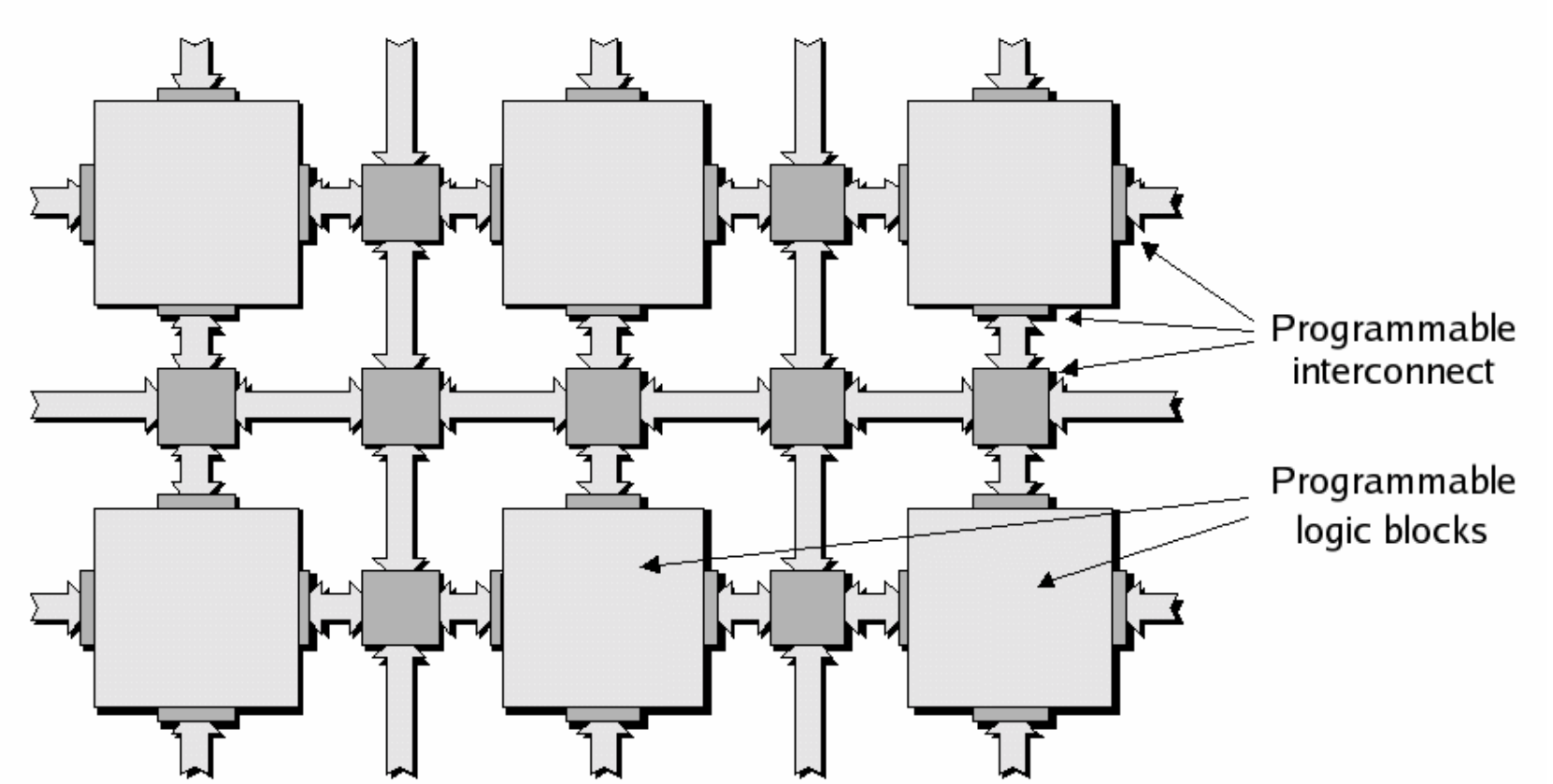
Commonplace Applications

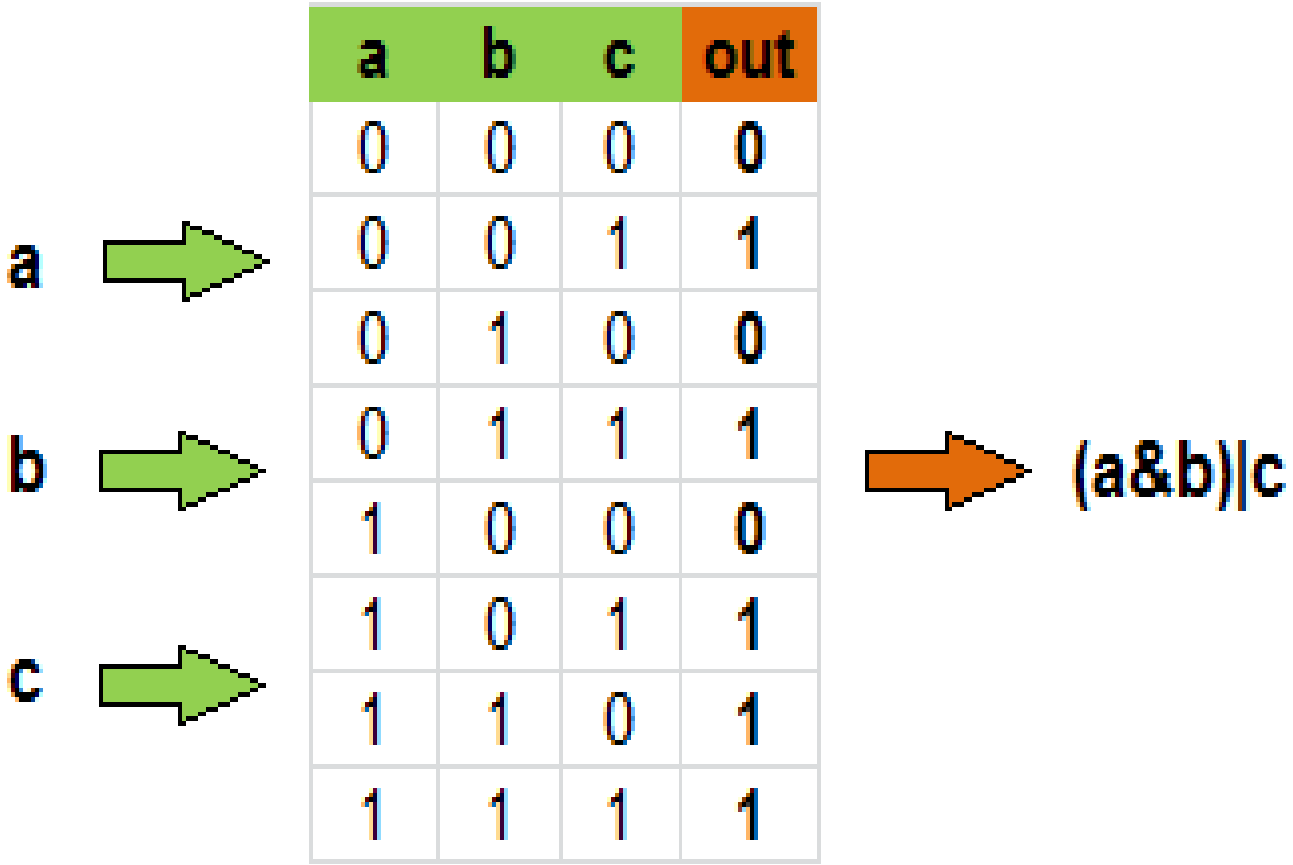
- Arithmetic Processing
- Communication Controller
- Coprocessor
- Crypto Processing
- Digital Signal Processing
- Video Processing
- ...

FPGAs

- Large array of configurable logic blocks (CLB) connected via programmable interconnects



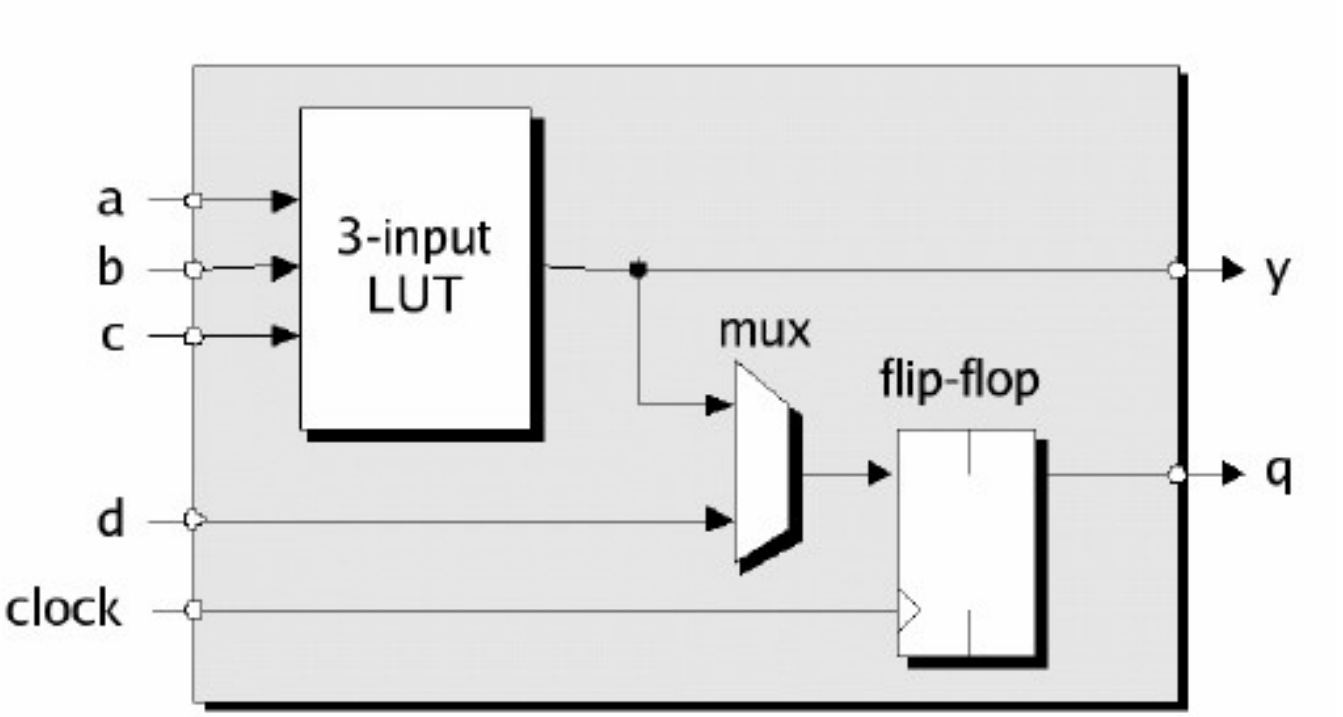
FPGA - elements - LUT



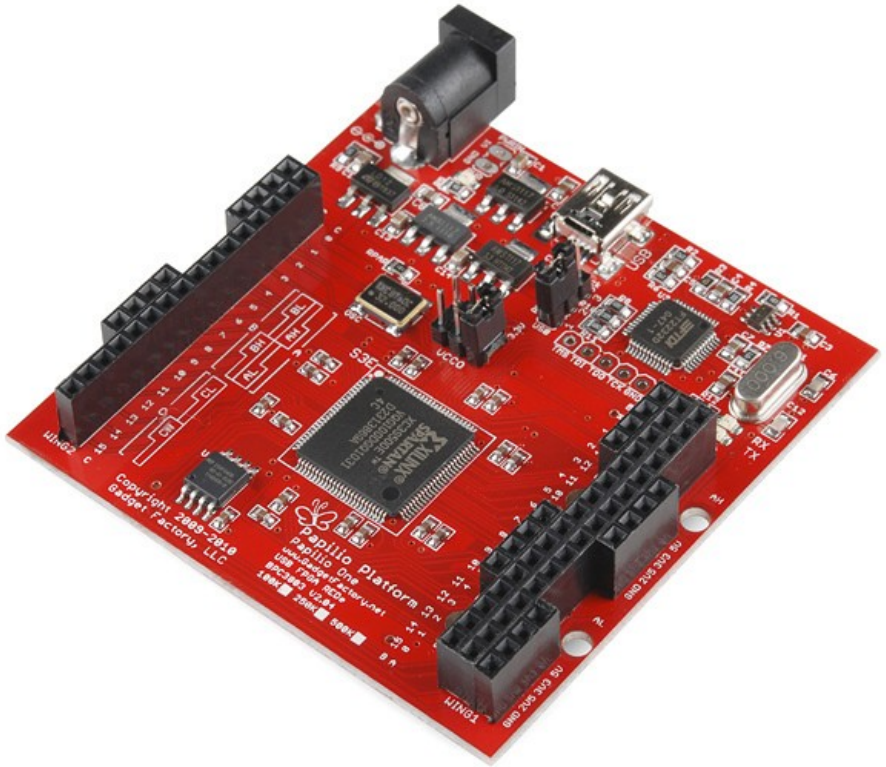
a	b	c	out
0	0	0	**0**
0	0	1	**1**
0	1	0	**0**
0	1	1	**1**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

A 3-input, 1-output LUT programmed to compute (a&b)|c.
Bits a,b,c are the LUT index, (a&b)|c are the stored values.

Logic Block Structure



Papilio One 250K

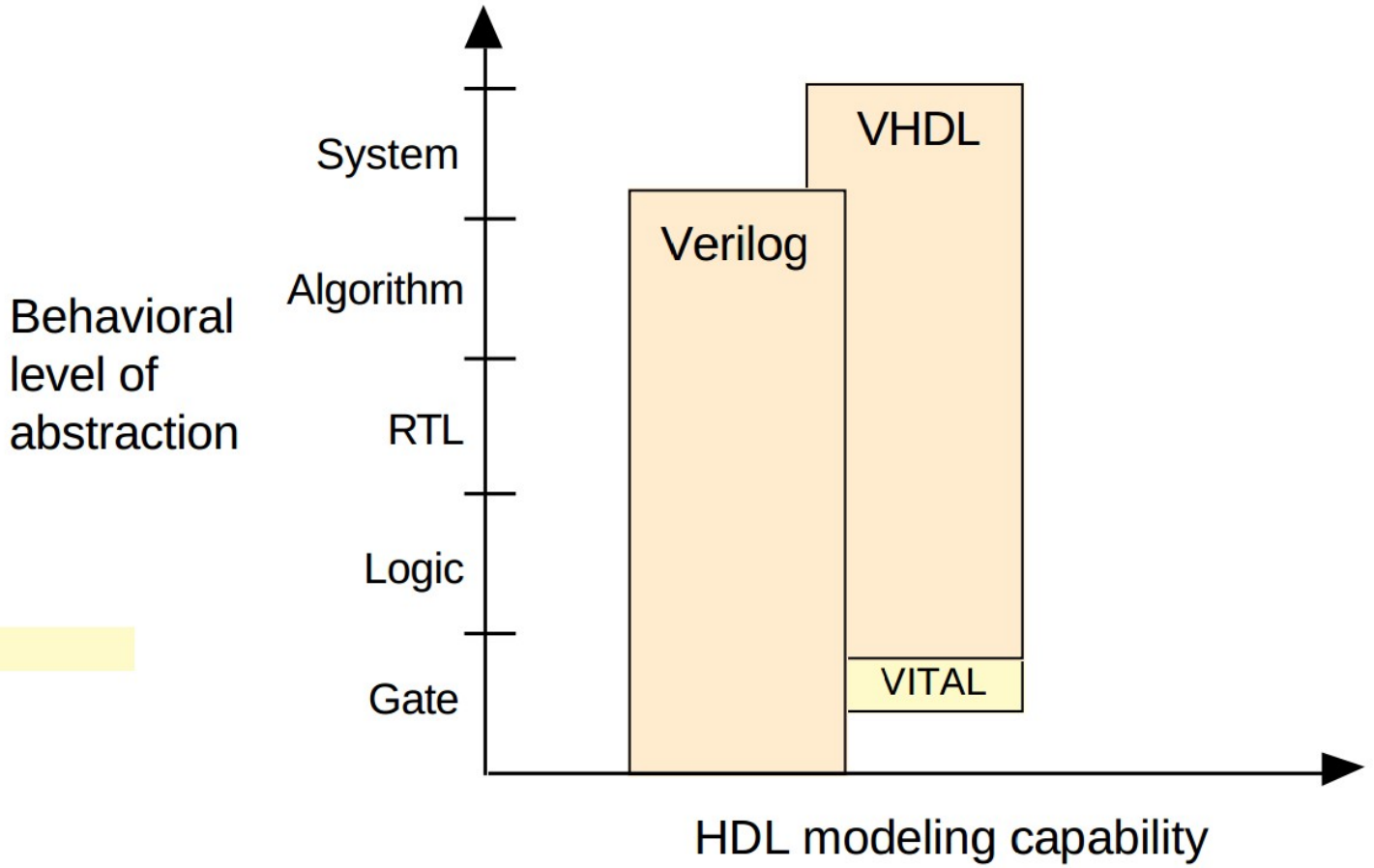


Spartan 3E FPGA
- 5,508 Logic Cells
- 1.2V, 2.5V, 3.3V
- 5Mhz – 300Mhz

Memory available:
- 192 Kbit of usable SRAM
- 4Mbit Flash chip

Design Languages

2 standardized languages: VHDL and Verilog.



Design Languages

	VHDL	Verilog
Type	Compiled	Interpreted with compiling possibility
Family	Ada	C, Ada
Typing	Strong	Weak
User-defined types	+	-
Dynamic memory allocation	+	-
Enumerated types	+	-
Modules	Packages	Include files

Examples

D Flip-Flop

VHDL

```
process (<clock>)
begin
    if <clock>'event and <clock>='1'
    then
        <output> <= <input>;
    end if;
end process;
```

Verilog

```
always @(posedge <clock>)
begin
    <reg> <= <signal>;
end
```

Synchronous multiplier

VHDL

```
process (<clock>)
begin
    if <clock>'event and <clock>='1'
    then
        <output> <=
            <input1> * <input2>;
    end if;
end process;
```

Verilog

```
wire [17:0] <a_input>;
wire [17:0] <b_input>;
reg [35:0] <product>;

always @(posedge <clock>)
    <product> <=
        <a_input> * <b_input>;
```

The End

Questions & Answers